VINEYARD
Versatile Integrated Accelerator-based Heterogeneous Data Centres

VINETALK FRAMEWORK RELEASED IN JANUARY 2018

FORTH announced the open source release of the VINETALK framework in a talk at the ENESCE workshop of HiPEAC 2018. The software is licensed under the Apache License v2.0.

VINETALK is a fundamental component of the VINEYARD stack as it addresses two main issues that are caused by the use of accelerators in datacenters. First, accelerators remain hard to use, and developers need to interface them with their applications through a diverse set of low-level APIs. Second, there is no mechanism today that enables sharing of accelerators, which is a common practice for reducing operating costs. VINETALK is a software tool that reduces the communication complexity between application software and accelerator hardware, and allows sharing of GPUs and FPGAs across applications. Furthermore, VINETALK allows applications to transparently access GPU, and FPGA accelerators, regardless of whether they run locally on a server, or in an Apache Mesos – managed cluster.

VINETALK consists of three major components:

1) A software interface, which exposes accelerators as task queues, called Virtual Access Queues (VAQs), to applications.
2) A software controller that implements a communication channel over shared memory and enables sharing of acceleration resources. It allows multiple processes to issue tasks and transfer data to accelerators.
3) A hardware interface, which simplifies the addition of new kernels by hardware developers.

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VINETALK can be found HERE

VINETALK

VINEYARD LEVERAGING FROM MAXELER'S NEW MAX5 DATAFLOW ENGINES

VINEYARD will be taking advantage from Maxeler's fifth generation DFE, MAX5 system, recently installed at VINEYARD's coordinator premises (ICCS), a further system will be also available to STFC soon. These systems will be used in the project to develop dataflow accelerated applications and as a testbed in the final evaluation.

The new DFE MAX 5 uses the powerful VU9P compute chip from Xilinx and sets a new standard in multiscale dataflow computing. MAX5 brings a 3-5x performance improvement and 2-3x increase in energy efficiency over previous generation MAX4 DFEs. Several leading customers have already upgraded their existing systems and are benefiting from its enhanced capabilities. MAX5 DFEs have been deployed in an HPC system at the Jülich Supercomputer Centre and are also being adopted by an increasing number of academic partners.

Last but not least, MAX5 DFEs are fully compatible with the Amazon EC2 F1 instances from Amazon Web Services. Maxeler supports the development and migration of applications to Amazon F1 with its MaxCompiler software.

VINEYARD JOINS ITS EFFORTS ON THE HETEROGENEITY ALLIANCE

VINEYARD has recently joined the Heterogeneity Alliance to collaborate with other projects and disseminate their results on the domain of heterogeneous computing. The alliance will focus on all phases of applications for Heterogeneous HW&SW to enable a new wave of development and execution tools for next-generation applications.

Heterogeneity Alliance goal is to join efforts of initiatives, like VINEYARD, interested in the development of future technologies and tools to advance, and take full advantage, of computing and applications using heterogeneous hardware (H-HW&SW). Its main goal is to create an association in which anyone can collaborate pursuing a common objective on supporting the creation of a common and an extendable set of technologies and tools (assets) around development for heterogeneous hardware, shared as open-source, which can be improved for mass adoption utilizing technologies.

Learn more about the Heterogeneity Alliance HERE

VINEYARD PRESENTS A PROGRAMMING FRAMEWORK AND RUNTIME SYSTEM FOR HETEROGENEOUS ACCELERATOR-BASED SERVERS

VINEYARD has developed a programming model for heterogeneous accelerator-based servers. The programming model can support acceleration of big data analytics frameworks such as Spark with hardware accelerators including Maxeler DFEs, general FPGAs, and GPUs.

The programming model provides a uniform interface for various accelerators. It offers multiple implementations of the same algorithm according to the accelerators and allows the programmer to invoke each implementation using the same interface.

VINEYARD has also developed a runtime system for using heterogeneous accelerators. For FPGA-based accelerators, VINEYARD has developed a framework that enables space-sharing of multiple applications on a single FPGA. This framework can distribute FPGA resources to each application dynamically according to the application's requirement by multi-kernel configuration-based task scheduling.

For the runtime system for GPUs, VINEYARD has developed FairGV, a GPU virtualization framework that can achieve ideal fairness and high utilization for GPU workloads. Leveraging FairGV, VINEYARD has developed three-level hierarchical scheduling methods for Spark workloads, which include Global, Local, and Application-level schedulers.

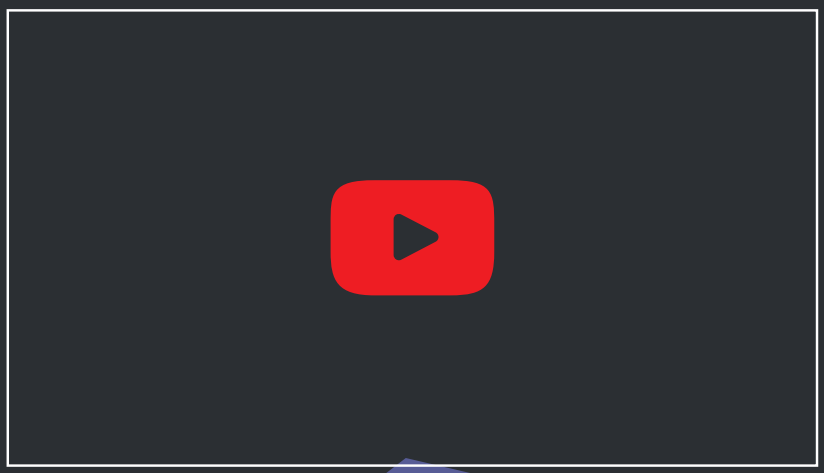
VINEYARD PRESENTS THE BRAINFRAME FRAMEWORK: BRAIN SIMULATION LIBRARY ON HETEROGENEOUS HPC PLATFORMS

VINEYARD aims to develop novel frameworks that will allow the efficient utilization of heterogeneous platforms from high-level programming frameworks and simulation platforms. One of the main frameworks that VINEYARD has developed is the BrainFrame. BrainFrame aims to allow the seamless deployment of several hardware accelerators (such as Maxeler's Dataflow Engines, FPGAs, and Xeon Phi) for highly efficient brain simulation.

The general goal of the project is to apply high performance, innovative solutions enabling large scale, accurate or real-time brain simulations and enhance experimental setups or data analysis of the experimental data concerning brain research. Thus, our activities employ a multitude of HPC and other technologies such as FPGAs, Dataflow Computing, GPUs and Many-core processors. The long-term goal and main focus of the effort within this theme is the development of a generic tooling framework for accelerated brain simulations, the BrainFrame Framework.

More information HERE

brainframe



VINEYARD WILL SHOW THE INTEGRATED FRAMEWORK IN STRATA 2018

LONDON, MAY 21-24

VINEYARD aims to present its latest results in the domain of heterogenous computing and data analytics acceleration in STRATA 2018. STRATA is firmly established as one of Europe's largest Big Data Conferences, attracting leaders in the big data space, from data scientists, analysts, developers, IT professionals, business leaders and entrepreneurs. STRATA London attracts over 2,250 conference delegates. In the STRATA Conference, VINEYARD will present the integrated framework for the acceleration of widely used frameworks like Spark and Storm using FPGAs and Dataflow engines.

Learn more HERE

VINEYARD will also present the latest works on 14th International Symposium on Applied Reconfigurable Computing (ARC) that will take place in Santorini in May 2-4.

Learn more HERE

PROJECT INFORMATION

VINEYARD – VERSATILE INTEGRATED ACCELERATOR-BASED HETEROGENEOUS DATA CENTRES

Start date February 1st, 2016

Duration 36 months

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Co-funded by the Horizon 2020 Framework Programme of the European Union under Grant Agreement nº 687628