VINEYARD
Versatile Integrated Accelerator-based Heterogeneous Data Centres

A RETROSPECTIVE OF AN EXCITING FIRST YEAR OF THE PROJECT

VINEYARD project aims to increase significantly the performance of Big Data applications and to reduce substantially the energy consumption of the data centre by allowing the seamlessly utilization of hardware accelerators in heterogeneous data centres.

During the first year, VINEYARD has managed to accomplish significant milestones towards the design of energy efficient data centres.

- VINEYARD has demonstrated the BrainFrame framework that allows the acceleration of neurocomputing applications on heterogeneous systems based on Xeon Phi and Dataflow engine accelerators. BrainFrame is a web-based interface that allows neuroscientists to speed up the execution of their applications by the seamlessly utilization of hardware accelerators.

- VINEYARD has also developed the VineTalk framework. VineTalk reduces the programming effort associated with FPGA-based accelerators and FPGA virtualization. VineTalk has been integrated with the Xilinx SDAccel development framework and evaluated to the Kintex UltraScale FPGA. The preliminary evaluation with a use-case of financial applications shows that VineTalk can offer effective FPGA sharing introducing marginal overhead to application execution time.

- VINEYARD has also released the SPynq framework: SPynq is a framework for the efficient mapping and acceleration of Spark applications on heterogeneous MPSoC FPGAs, such as Zynq. SPynq allows the seamlessly utilization of the programmable logic in heterogeneous MPSoCs for the hardware acceleration of computational intensive Spark kernels, and in a use case scenario based on logistic regression it can achieve up to 52x speedup compared to an x86 processor.

- VINEYARD has also developed several hardware accelerators that can be used as IP cores for heterogeneous data centres. Specifically, it has developed a hardware accelerator for financial application that can offer up to 300x speedup, a hardware accelerator for logistic regression that can offer up to 56x speedup and a hardware accelerators for Inferior-Olive Nucleus simulation that can offer up to 30x speedup.

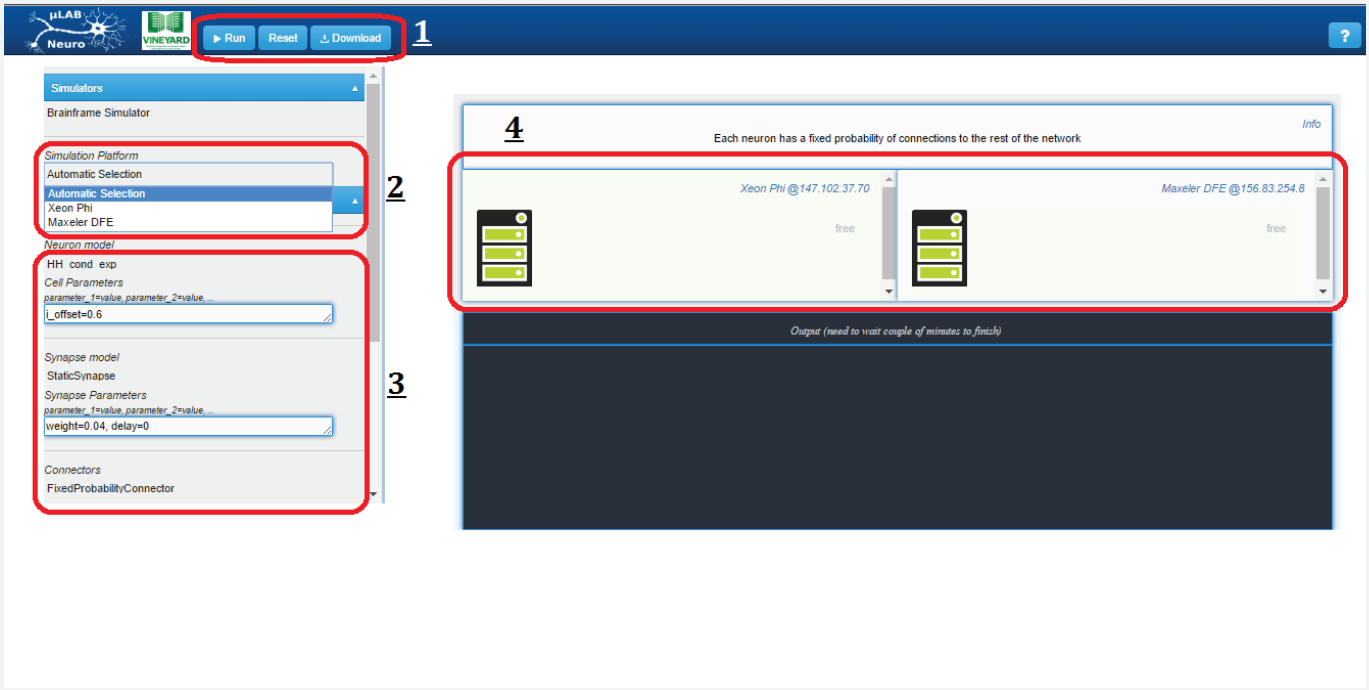
Dr. Christoforos Kachris and Prof. Dimitrios Soudris
(ICCS - Institute of Communications and Computer Systems)

BRAINFRAME WEB-BASED FRAMEWORK FOR ACCELERATION OF NEUROCOMPUTING APPLICATIONS

In the context of the VINEYARD project, Neurasmus and ICCS have developed the BrainFrame framework in order to take advantage of heterogeneous ensembles inside datacentres.

The framework's first goal is to accelerate the simulation of large, complex neuronal networks, relevant to current neuroscientific research at unprecedentedly short simulation times through transparently using different accelerators. The second, but equally important, goal is to provide a familiar and easy frontend for the neuroscientists that hides the complexity of heterogeneous acceleration, without requiring the constant mediation of a hardware/ software engineer for achieving acceleration.

The user (neuroscientist) initially sets up the characteristics of the neuronal network and decides on the simulation parameters through an intuitive Web GUI. Also, the user has the option to a priori determine the platform that the simulation will be executed on. The webserver then passes the user-provided info onto the PyNN framework, which makes the final choice of accelerator type based on a number of parameters (to be analysed later). Finally, when the simulation has ended, the results are sent back to the Web GUI.



BrainFrame Web GUI.
A DEMO video of the BrainFrame framework is available HERE.

The image above is a screenshot of the web GUI, with the most important elements highlighted. The user / neuroscientist will:

- Select the platform that the simulation will run on: Xeon Phi, Maxeler DFE or Automatic selection (Area 2). The available resources on the heterogeneous ensemble are shown in *Area 4.*

- Select the neuronal simulation models and parameters (Area 3):
  - The neuron model along with the model parameters.
  - The plasticity mechanism, if any, or static synapses.
  - The connections of the neuronal network and their parameters.
  - The number of neuron cells and the simulation time of the network.

- Finally, run the simulation from the Actions buttons in Area 1, and download the results or reset the simulation options.

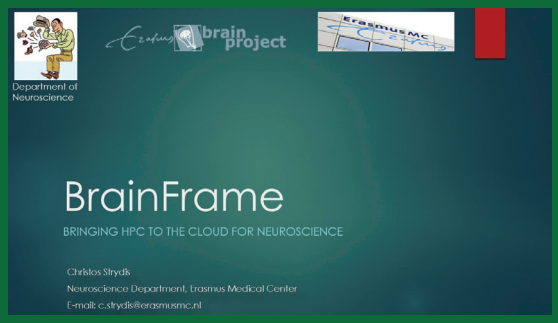
POSITIVE REACTION TO BRAINFRAME FROM STAKEHOLDERS

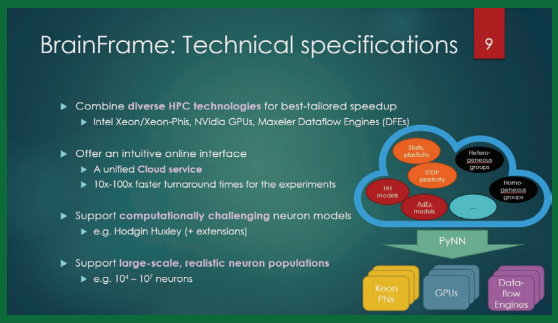
The BrainFrame web service was presented by Dr. Christos Strydis at an annual lab talk of the Neuroscience Department in the Erasmus Medical Centre, on 18 of April 2017.

The presentation addressed the benefits of heterogeneous computing for neuroscience and included a live demonstration of the web service to the audience.

Various attendees requested for various simulation runs and were able to see the results being generated on the fly!

Overall, the reception of BrainFrame was high and interest has peaked.





Mr. Harry Sidiropoulos and Dr. Christos Strydis
(Neurasmus)

Cover page and sample page of lab talk

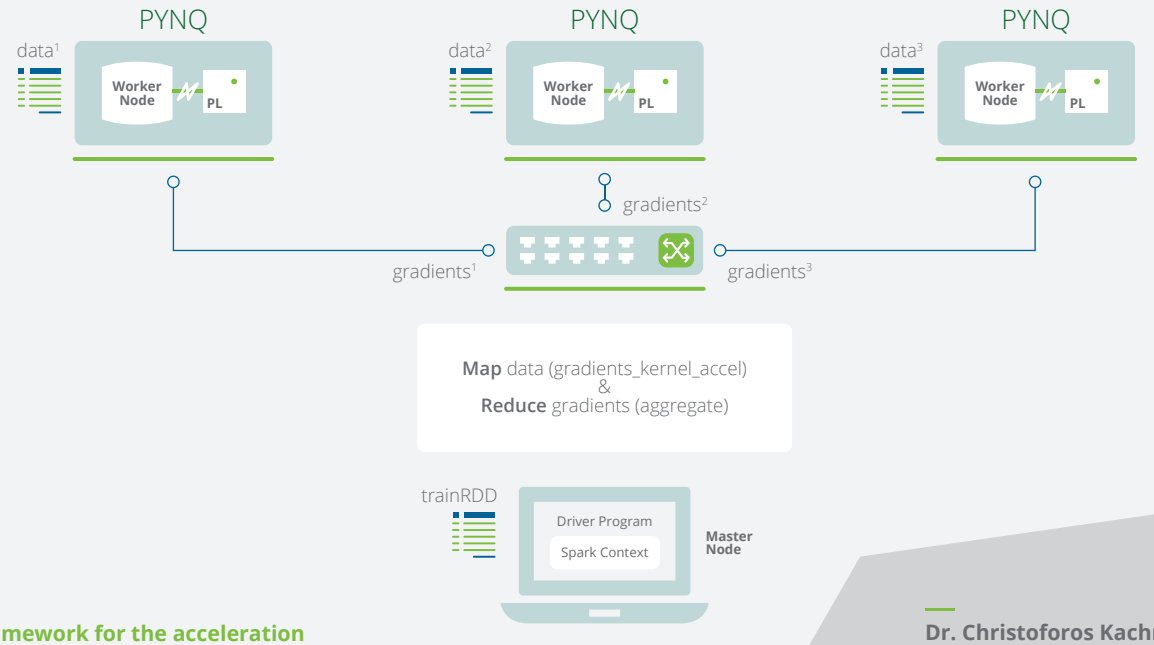
VINEYARD GITHUB ON SPARK ACCELERATION IN THE PYNQ DEVICE

Spark is one of the most widely used frameworks for data analytics that offers fast development of applications like machine learning and graph computations in distributed systems.

VINEYARD has recently released the SPynq framework. SPynq is a framework for the efficient mapping and acceleration of Spark applications on heterogeneous MPSoC FPGAs, such as Zynq. Spark has been mapped to the Pynq platform and the proposed framework allows the seamlessly utilization of the programmable logic for the hardware acceleration of computational intensive Spark kernels. VINEYARD has also developed the required libraries in Spark that hides the accelerator's details to minimize the design effort to utilize the accelerators. On the reconfigurable logic part, the hardware accelerators for the specific application are hosted. The hardware accelerators are invoked by the python API of the Spark application. Therefore, the only modification that is required is the extension of the python library with the new function calls for the communication with the hardware accelerator.

SPynq has been evaluated in a typical machine learning application based on logistic regression. The logistic regression kernel has been developed as a Pynq overlay and incorporated to the Spark. The performance evaluation shows that the heterogeneous FPGA-based MPSoC can achieve up to 53x speedup compared with a x86_64 laptop system. The proposed system can also offer reduced energy consumption and can also reduce significantly the development time of embedded and cyber-physical systems on Spark applications.

The SPynq framework is available to download and try in the following Github HERE



SPynq framework for the acceleration of Spark applications based on the heterogeneous Pynq MPSoC platform.

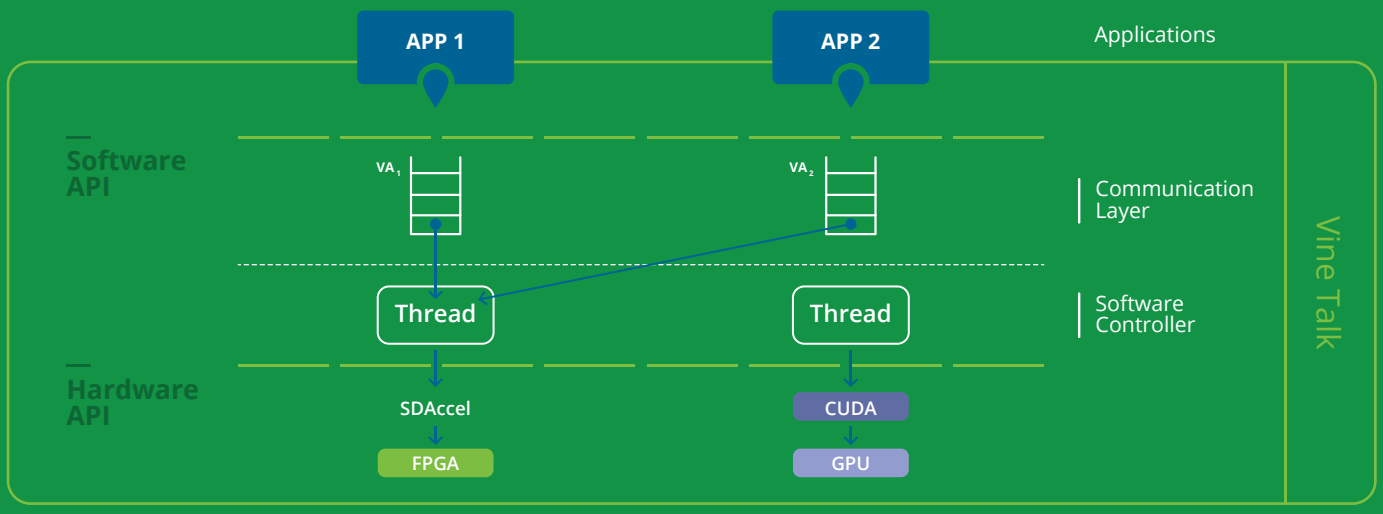
Dr. Christoforos Kachris
(ICCS - Institute of Communications and Computer Systems)

VINETALK INTERFACE AND THE INTEGRATION WITH OUR SYSTEM FOR THE ATHENS STOCK EXCHANGE MARKET

FPGA-based accelerators are becoming a first-class citizen in data centres.

Adding FPGAs in data centres can lead to higher compute densities with improved energy efficiency for latency critical workloads, such as financial applications. However, deployment of FPGAs in datacentres is hindered, as both developers and cloud providers face difficulties. Application writers need to deal with FPGA interfacing as well as application logic/algorithms. At the other hand, cloud providers are reluctant to deploy FPGAs in large scale, due to the FPGAs lack of sharing that results in reduced utilization and questionable ROI.

To address this problem, VINEYARD introduces VineTalk, a framework that reduces the programming effort associated with FPGA-based accelerators and FPGA virtualization. Specifically in the context of financial applications, VINEYARD has integrated VineTalk with the Xilinx SDAccel development framework and mapped it to the Kintex UltraScale FPGA. Our preliminary evaluation with a use-case of financial applications shows that VineTalk can offer effective FPGA sharing introducing marginal overhead to application execution time. In our evaluation, we use three financial kernels: Black&Scholes, Black-76, and Binomial. Our results show that VineTalk reduces both programmer effort at the application level by reducing lines of code related to kernel invocation by about 30% with significantly simpler semantics and introduces over- head between 0.9% and 4% compared to native application execution over the FPGA. Finally, VineTalk provides the ability of accelerator sharing from consolidated applications, with less than 2% overhead.



Design overview of VineTalk and the use of virtual accelerators (VA) to abstract physical resources.

Angelos Bilas
(FORTH)

VINEYARD IN HIPEAC2017

STOCKHOLM, JANUARY 2017

VINEYARD participated in the HiPEAC 2017 conference, where it had the chance to present two papers one in the Workshop on Reconfigurable Computer (WRC) and another in the Workshop on Energy-efficient Servers for Cloud and Edge Computing (EnESCE). The EnESCE workshop was co-organized by the projects VINEYARD, dRedBox, M2DC and Uniserver.

The goal of the workshop was to present the most recent work on next generation energy-efficient servers and foster the interaction between the universities, research centres and industry that work on this field. Besides the technical paper, two keynote talks were given: one from Andreas Oloffson from Adapteva and one from Peter Pietzuch from Imperial College.

The following papers were presented in the WRC and the EnESCE workshops respectively:

- **High Level Synthesis versus HDL: A Case study on Hardware Accelerators for Financial Applications**, Ioannis Stamoulias, Christoforos Kachris, Dimitrios Soudris.
- **Hardware acceleration of Spark:** A use-case on all-programmable MPSoCs Christoforos Kachris, Elias Koromilas, Ioannis Stamelos, Dimitrios Soudris

VINEYARD'S PAPER "SPARK ACCELERATION USING PYNQ FPGA" WAS AWARDED BEST STUDENT PAPER AT MOCAST 2017

On the 4 - 6 May 2017, VINEYARD participated in the International Conference on Modern Circuits and Systems Technologies, MOCAST 2017, in Thessaloniki.

The Conference brought together leading academic and industrial scientists and researchers to exchange and share their knowledge and experiences about all aspects of Circuits and Systems.

At the MOCAST conference, VINEYARD's paper on "Spark acceleration using Pynq FPGA" was awarded best student paper.

More information about the event HERE

UPCOMING EVENTS

ISC HIGH PERFORMANCE 2017

18 - 22 June 2017 | Frankfurt, Germany

From the 18 to 22 of June 2017, the conference "ISC High Performance 2017" will be organised in Frankfurt, Germany.

The conference will focus on the technological developments in high performance computing and its application in scientific fields, as well as its adoption in commercial environments.

On Monday (19th of June) from 15h to 20h, VINEYARD project will be in the exhibition area at the HiPEAC booth A1430, where VINEYARD will demonstrate the BrainFrame for high performance neurocomputing application in heterogeneous architectures and the Spark on FPGA acceleration framework called Spynq.

More information about the event **HERE**

PROJECT INFORMATION

VINEYARD – VERSATILE INTEGRATED ACCELERATOR-BASED HETEROGENEOUS DATA CENTRES

Start date February 1st, 2016

Duration 36 months

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